VSM (Virtual Synchronous Machine) Control System Design, Implementation, Performance, Models and Possible Implications for Grid Codes

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***Abstract*— Recent system level studies, have shown that the use of Grid Forming control schemes such as the Virtual Synchronous Machines (VSM) for grid connected power convertors offer significant benefits enabling increased penetration of convertor based generation.**

However, many of these studies have employed a simplified model for the power converter and its control system to enable large-scale power systems to be efficiently simulated. For example, "RMS" models for convertors can mask some of the behavior of the power convertor during abnormal and fault conditions.

This paper will present the development of a VSM controller for a 17kVA battery energy storage system. The response of this experimental system to a step load change is shown. The paper focuses on the VSM algorithm, power and current limiting modes of operation.

It will also discuss how the algorithm is implemented both in the RMS model and real convertor. RMS models are of considerable importance to system operators such as NG ESO, as they are currently favored methodology for whole system studies. The paper will also discuss accurate models to the appropriate level of detail and some of the differences between the RMS and switch level models / physical implementation.

Keywords-component; Grid Forming Convertors (GFC), Virtual Synchronous Machine (VSM), RMS Modelling, Current Limit, Power Limit, GC0100, Grid Codes (GC), Inertia.

I. INTRODUCTION

This paper is the second of five papers describing National Grid's two VSM (Virtual Synchronous Machine) NIA (Network Innovation Allowance) projects. These two projects have been undertaken in partnership with University of Nottingham (UoN) and University of Strathclyde (UoS). They are intended to improve the understanding of the implications of GFC proposals addressed through GC0100 Option 1 [9] and subsequently the VSM Expert Group [8].

The purpose of the projects and/or papers are:

1. To design and test a VSM algorithm in line with general GFC/VSM principals such as GC0100 option 1 [9].
2. To establish which plant control principals, parameters and tests are particularly relevant to grid stability.
3. To understand how grid forming performance affects one of the possible convertor designs and strategies which might mitigate any negative effects.
4. To establish whether it is possible to provide grid forming performance from hybrid solutions (for example STATCOMS) where not all of the converters are grid forming.

It should be noted that whilst the authors have sought to explore a possible implementation of VSM. It is not National Grid's intention to mandate any specific design. NG ESO (National Grid Electricity System Operator) only seeks to examine some of the practical considerations surrounding the technical requirements detailed in [9] and [8]. This is not intended to prescribe a design of a physical convertor, it is intended to simply illustrate one potential approach for discussion though it is noted that some other implementations could be used some of which are also discussed in the papers.

It is suggested readers first read [1] to get a broader introduction conclusions on the topics and controller models presented in this paper and the other papers.

Fig. 1 below shows the overall block diagrams of the controllers implemented by NG ESOs partners UoN and UoS. The implementation of the controllers and associated hardware differ slightly as each partner focused on different aspects of the design.

The numbers [2] [4] etc. in Fig. 1 indicate where specific topics are covered by specific papers and [*] refers to this paper.

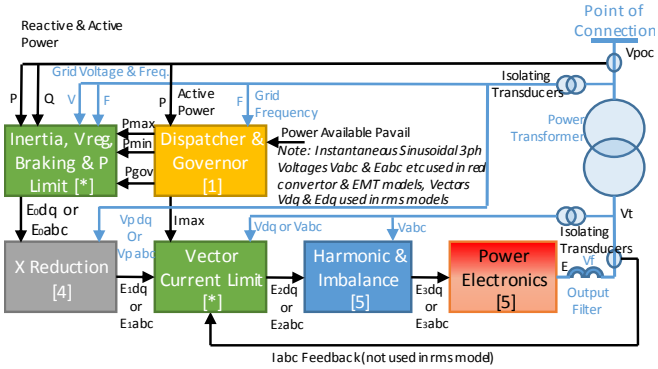

Fig. 1 – Simplified Block Diagram of a potential VSM Implementation

From Fig. 1 we can see the converter design largely consists of 6 major blocks:

- Dispatcher and Governor
- VSM (Inertia simulation and stabilizing, Dynamic braking, Voltage Control and Power Limiter).
- Impedance Reducer
- Vector Current limiter
- Harmonic and Imbalance Management
- Convertor Output Stage and Power Electronics

This paper focuses on the second and fourth items, the core VSM algorithm and the vector current limiter. It will discuss the implementation of the algorithms in the context of stability pathfinder [11] [12] and the GC0100 option 1 [9] highlighting key design decisions.

II. Introduction VSM Algrorithm

The VSM algorithm presented here is based on the earlier work published in 2016 [2] [6]. The work in 2016 used MATLAB and PowerFactory RMS models to demonstrate the potential benefits of VSM. This work has now been successfully replicated and enhanced using real convertors connected to both test networks and a live distribution system.

In this section, the key features of the 2016 algorithm will be reviewed and then we will discuss some of the enhancements and options which have been added and have resulted from the work presented here. The paper will also discuss the practical implementation of the algorithms and where they differ from the implementation in RMS models.

The original VSM algorithm presented at the Wind Integration Workshop in Vienna in 2016 [2] consisted of:

1. Droop (FSM) Governor
2. Inertia Simulation
3. Damping (3 methods were discussed)
4. Dynamic Braking
5. Droop Voltage Control
6. Slip (RMS simulation) / 50Hz (MATLAB simulation) Output Oscillator
7. Power Limiter
8. Scaler / Reactive Current Limiter

The design has been enhanced in the following ways. First the governor has been improved and now provides FSM and LFSM modes and is described in Paper 1 [1]. The inertia simulation is basically the same although an additional damping method has been added.

Dynamic braking has been extended to the power limiter, a block diagram of which is presented in this paper and the various merits or otherwise of different strategies are discussed.

The current limiter is considerably enhanced. The original current limiter is referred to here as a scaler and reactive current limiter. It consisted of two systems, one of which attempted to limit the AC voltage across the output filter and hence limit the AC current. In addition, there was a system which reduced the output voltage of the convertor if reactive current exceeded a predetermined level.

The current limiter presented in this paper is referred to as a vector current limiter, unlike the original, it's capable of dealing with both short circuits and vector shifts / angle changes. This current limiter has significant benefits as it injects current attempting to restore the voltage vector back to its correct location in much the same way as synchronous machines do but at reduced current i.e. within the convertors current rating.

III. VSM Algorithm

A. *Extended Operating Range*

GC0100 option 1 [9] requires that grid forming convertors have the ability to provide extended short time rated operation outside of their continuous operating range. Fig. 3 below shows the extended operating region as originally proposed in GC0100 option 1 [9].

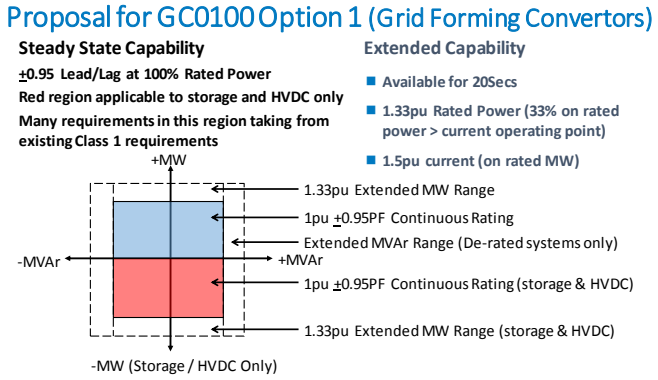

Fig. 3 – GC0100 Extended Operating Range for GFC

It was originally proposed that equipment should be capable of operating in the extended region for up to 20 seconds, however in paper 1 [1] we have discussed more conservative and reduced timescales and more flexible operating regimes where the additional power may be obtained from storage or reducing output or a combination of both.

During consultations on GC0100, NG ESO indicated that whilst there is a requirement for the extended operating range, the net output over the longer term is not increased and that any operation in extended region would be followed by subsequent operation at lower output when the frequency

recovered. This allows for repeated operations as storage components can recharge as the frequency increases.

HVDC owners indicated that the increase in rating is likely to be reflected in the convertor cost. It has therefore been proposed that there should be an option to de-rate by up to 25% when it is necessary to run Grid Forming Mode which would allow for the 33% headroom on rating (25%/75% = 33% headroom).

In addition to the above there has been some discussion as to whether the additional 33% overrating is required on the reactive range or whether it is only required for active power, as this potentially affects the rating of other components such as the parallel diodes across the transistors.

For systems which are derating this capability should be incorporated in the design and therefore available. However, for systems which have installed the additional equipment it is likely it will increase the cost and there is therefore a reduced requirement.

B. Voltage Source Over the Frequency Range 5Hz to 1kHz

GFC's are effective at stabilizing power systems because they operate as voltage source behind an impedance. During and after an event (typically a fault and / or switches opening or closing e.g. generator or line trip, load change or auto re-closer) the GFC attempts to maintain the same AC voltage level, phase angle and frequency or only slowly modulates them (provided the device remains within the extended rating). Even if outside the extended rating, GFC will attempt to restore the voltage to the correct phase whilst remaining within rating e.g. during faults.

Under changing network conditions, AC voltage sources which maintain largely constant voltage, phase angle and frequency, change output current to accommodate the change in network topology or operating conditions. Furthermore, the current which flows is determined by the network itself and not the convertors control system, the only exception to this being when the convertor rating (power, reactive power or current) is exceeded and limiters take control to prevent excessive currents or power, which might otherwise damage the convertor.

It therefore follow's that accurate definition of this behavior should be captured by any GFC related Grid Code. GC0100 option 1 indicated that the convertor should operate as a voltage source over the 5Hz to 1 kHz band. This definition was chosen because it doesn't prohibit the use of an inner current loop but does require such a control loop to operate at a bandwidth higher than 1 kHz. Likewise, it requires that the pulse width modulation or voltage steps of the output transistors is updated at least 2000/second irrespective of whether the output stage uses direct pseudo voltage control of the PWM waveform or an inner current loop, in which case higher switching frequencies might be required.

As many convertors now switch at or above 2 kHz (e.g. with both edges being controlled), a 1 kHz upper bandwidth was considered practical and achievable. Typically, such devices have filter impedances of the order of 10% for 2 kHz operation with less being required at higher frequencies.

1 kHz was specified as the upper limit because it also has the benefit of avoiding and mitigating the most dominant prime harmonics i.e. 5th, 7th, 11th, 13th, etc. as voltage source convertors will attempt to act as an active filter and sink harmonics within their frequency band. Higher frequencies, in the kHz region, don't typically propagate as far across the network as they tend to be damped down by series reactance and parallel capacitance and where they might be troublesome are typically dealt with using passive filters.

With current loops being permitted at greater than 1 kHz the impedance can be simulated in software and the apparent voltage source may be moved from the transistors themselves to some point further into the filter circuit for example. Fig. 4 below shows two different GFC voltage source implementations.

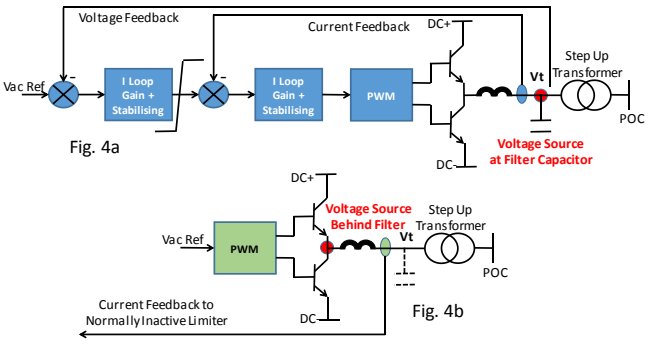

Fig. 4 – Alternative Voltage Source Implementations

Fig. 4b shows the implementation used here which relies on normally passive / inactive current and power limiters (see [2] and following text) which normally have no effect on the signal from the output oscillator. The output oscillator signals are converted into a PWM (Pulse Width Modulation) signal which from the other side of the filter looks like an AC voltage.

Fig. 4a shows an implementation where the pseudo voltage produced by the PWM is used to control the current feeding the capacitor which develops a voltage behind a transformer or other impedance. This system uses the inner current loop, which is always active, to both limit the output current and generate and control the voltage on the output capacitor.

Both 4a and 4b require that a low pass passive filter is fitted with a bandwidth of less than 1 kHz which ultimately ensures that the switching frequencies and in the case of 4a high frequency controller actions are significantly attenuated and are not observable on the network to which the convertor is connected. In the case of 4a the inner current loop would have to operate at a speed which ensured its bandwidth was above 1 kHz.

C. Output Oscillator and Lower Bandwidth Limit of 5Hz

Fig. 5, shows the output oscillator as represented in the PowerFactory RMS model. In the real convertor, it is simply a 3ph sin wave oscillator, however in the RMS modelling tool it is represented as slip oscillator, the frequency of which is the difference between the nominal and actual grid frequency.

At nominal frequency (50Hz) the RMS modelling tool represents the voltage at the bus bar as an AC vector with real and imaginary components which are static. In the

implementation used here, when the frequency changes, the vector starts rotating at the slip frequency.

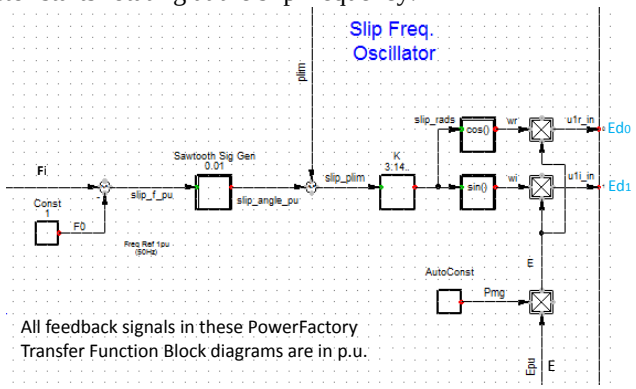

Fig. 5 – Output Oscillator

The output oscillator is controlled by two primary signals, one setting the frequency and the other internal voltage level of the convertor, referred to as E or E_0, E_1 etc. (see Fig. 1). E is the voltage behind the filter reactance, Vt is the terminal voltage on the other side of the filter (see Fig. 1).

The lower bandwidth limit of 5Hz applies to the control signals which control the output oscillator frequency and amplitude. 5Hz was chosen as it is used commonly in other parts of the GB GC [10] to prevent interaction with conventional machine rotor resonances. The topic of shaft oscillations and interactions is discussed in various papers and although the GBGC mandates 5Hz, the IEEE Guide for Excitation Systems [7] indicates shaft oscillation frequencies extend down to 4 Hz.

D. Inertia Simulation, Damping and Dynamic Braking

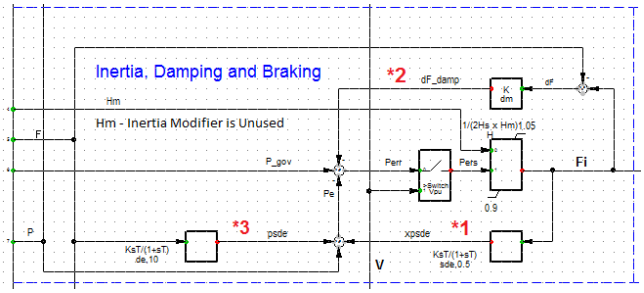

Fig. 6 – Inertia Simulation and Dynamic Braking

Fig. 6 shows the basic configuration of the inertia simulation for this VSM based design. The design is largely unchanged from the design presented in [2]. It consists of an integrator term 1/2Hs which simulates the inertia. Its output signal is frequency in p.u. and its input is the difference between the power signal from the governors and the active power measured at the output from the convertor both in p.u.

The summing junction(s) which determines the difference or sit on route of the signals also add in the various damping signals which have been included for evaluation. The main damping terms are denoted by *1 and *2 on Fig. 6. The first signal has generally been used in National Grid and Strathclyde University and the second by Nottingham University. Both work and are zero under steady state conditions. *1 uses a differential term to remove the steady state component and *2 subtracts the feedback frequency from the output frequency of the inertia simulation. The other two, *3 and *4 (see Fig. 7) are as presented in [2] and have not generally been used but can be used in combination with the others.

Between the summing junctions and the 1/2Hs block is the braking switch which operates as described in the 2016 paper [2] but as its function is critical, it will be explained again. This switch opens if the terminal voltage of the convertor drops below 0.85pu. This makes the inertia infinite under fault conditions stopping the convertor from changing its frequency, which is equivalent to fitting the perfect quantity of breaking resistors to a Synchronous Machine (SM), under fault conditions. It is believed to incur no or little cost and reduce the rating requirements on the convertor as explained in the 2016 paper [2].

With the damping set to typical levels for a SM and without the breaking switch the convertor would swing like a SM and for a 140ms fault the devices power might briefly double. This is undesirable for both the convertor and the power system in general, hence the need for the breaking switch or other measures to damp out such a swing. GC0100 option 1 specified the inclusion of braking.

E. Voltage Controller

Fig. 7 below shows the voltage controller which simply comprises of a basic reactive voltage controller with reactive power droop as presented in [2]. It contains a 1/(1 + sTf) block which has a similar effect to the field time constant of a SM but most importantly serves as a low pass filter to ensure the 5Hz lower bandwidth limit is maintained.

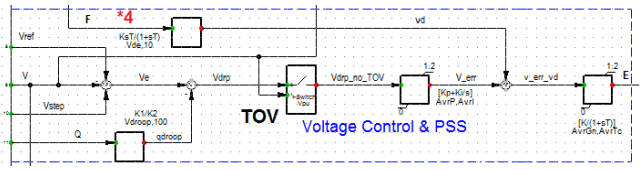

Fig. 7 – Voltage Controller

The output filter is fed from a PI controller which amplifies the error signal under dynamic conditions. The integrator term zero's out any steady state error for normal continuous operation and allows the proportional term to be reduced as it is only needed for dynamic responses. An additional stabilizing signal *4 vd, is available as described in the 2016 paper [2] but it has not been used because like a PSS (Power System Stabilizers) on a SM it modulates the volts and to date we have not found it necessary.

The only significant change is the inclusion of the optional TOV (Transient Over Volts) switch, which acts in a similar manor to the breaking switch in the inertia simulator, preventing the integrators from winding up during the fault i.e. when the volts drop below 0.85pu. This has the benefit of reducing the transient over voltage post fault, although it should be pointed out that with the correct settings i.e. a long filter time in 1/(1 + sTf), this typically isn't an issue as there is only a small increase in post fault voltage.

F. Power Limiter

Fig. 8 below shows the block diagram of the power limiter. Its output signal is normally zero but can rapidly increase or

decrease to +1 or -1 representing ±180 degrees, although it is normally limited to ±90 degrees. The output signal is added to the output of the slip oscillator / 3ph oscillator (rms model / real convertor respectively).

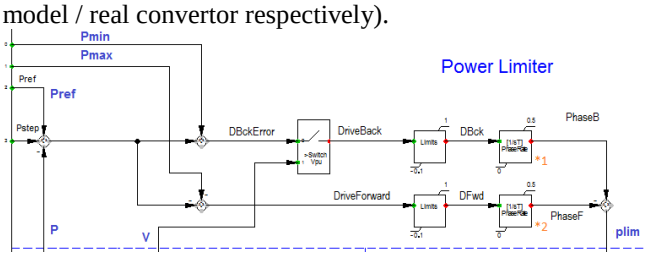

Fig. 8 – Power Limiter

The output signal is generated by two integrators, one for limiting increases in power, the other for limiting decreases in power. These limiters are fed from two error signals which are calculated from the difference in measured power output and the limiter set points. The low-level power limiter has a braking switch with identical setting to those used by the braking switch discussed earlier. This prevents the power limit activating during faults.

G. Continuous vs One Shot Power Limiter

The authors of the paper considered publishing an alternative power limiter where the limits on the integrators marked *1 and *2 in the Fig. 8 are removed. This has the following perceived benefits:

1. There is no need to slowly wind back the integrators after the power limiter has operated
2. It allows the convertor to continuously rejected the over power condition without relying on the current limiter potentially providing additional convertor protection

For convertor manufacturer's, the above advantages might lead them to implement power limiters which allows this mode of operation either using the above method or by some other e.g. returning to PLL (Phase Lock Loop) control. However, the following text debates the subject further and indicates a potential flaw in this approach, although it is accepted further studies are required.

Consider a scenario for an event where the total available power overhead of all the convertors, at a system level is exceeded e.g. an islanding event is so large that the low frequency island must shut down or partially shut down e.g. a loss of generation so great that not only are the frequency response reserves exceeded but in addition inertial reserves are also exceeded.

If this system is operating with only a few remaining SM's, the convertors are potentially in a position to continuously vector shift, limiting their active power whilst maintaining reactive support and hence maintaining the system volts.

Under these circumstances, depending on configuration, it might be possible to push the power imbalance onto the remaining SM's. Without performing studies it's unclear what the impact of this might have on SM's but possible outcomes might include pole slipping, limiting behavior and voltage collapse or extended duration high power output.

Such circumstances are extreme and unlikely, leading to full or partial system shutdown, however Grid Codes and the requirements that result from them might wish to consider this scenario. The purpose of this text is therefore to open a debate regarding convertor fast angle changes. Should convertors fast angle changes be limited in range, should they be unlimited or should this be at the discretion of the SO/TSO?

H. Current Limiter RMS Model

Fig. 9 is a vector diagram showing the relationship between the terminal voltage of the convertor its filter impedance and its internal voltage E_1 created by the output oscillator. For simplicity, assume the X Reducer (see fig. 1) is off and has no effect, as under these conditions $E_1 = E_0$, the oscillator output.

The AC current produced by the convertor is proportional to the difference between the two voltages Vt and E, which under normal circumstances is equal to E_1 (refer to Fig. 1 for Vt, E_1 and E in the block diagram). δ represents the operating angle and is equivalent to the rotor angle in a SM, θ is Power Factor angle. The length of Vt (not drawn to scale here) is proportional to 1/Xf at nominal volts where Xf is the filter reactance. Similar diagrams are also discussed in papers 3 [3] and paper 4 [4] in relation to the impact in OFTO networks and strategies improving grid forming performance.

The maximum AC current that can be produced by the convertor is represented by the concentric circles where the inner circle is the maximum continuous rating and the out circle the 1.5x short time rating. During a fault Vt typically reduces and its phase δ, may also change. Vtf shows a change in both level and phase relative to E_1 the reference oscillator, because of the fault. This results in a new current Iff where Iff = Vff/Xf i.e. voltage across the filter, divided by its reactance. Because of the braking described earlier in this paper, E_1 remains at the same frequency and magnitude as before and if unrestrained Iff would exceed the convertor fault current rating Ifl. The AC filter voltage therefore needs to be constrained to Vfmax where Vfmax = Ifl.Xf.

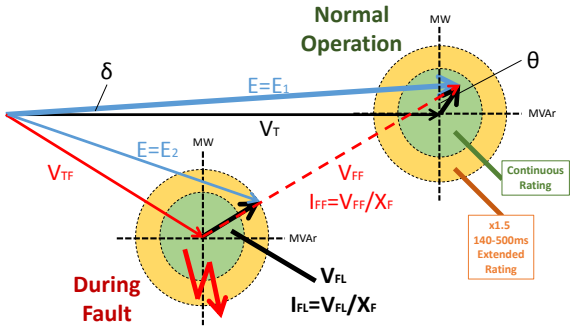

Fig. 9 – Vector Current Limiter Phasor Diagram

Fig. 10 below shows the RMS block diagram of the current limiter algorithm which limits the output current to Ifl, the convertor fault rating. This is achieved by deriving the vector voltage across the filter (Vfr and Vfi) and dividing it by the scalar quantity Vf. The equivalent resulting vector (Vfd and Vfq) if converted a scalar quantity, is always 1 or less than 1

for very low convertor output due to the limiter *A, which simply prevents divide by zero errors. This quantity is multiplied by the maximum permissible AC filter voltage (Vfmax) which is derived by multiplying Imax by the filter reactance. This is then added to Vd and Vq. If an over current condition occurs i.e. Vfmax is exceeded (see *B), switches *C operate and the convertor outputs vector E_2 which is set to produce the maximum allowed filter voltage limiting the AC current. See Fig. 1 for an explanation of E_0, E_1 and E_2, E_0 is the slip oscillator output, and E_1 the output of the X reducer, see [4], which when switched off $E_0 = E_1$ and $E_0d = E_1d$ etc.).

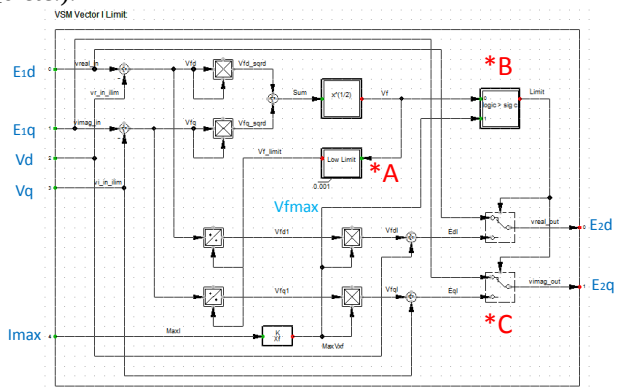

Fig. 10 – Vector Current Limiter Transfer Function Block Diagram for rms Modelling

IV. Vector Current Limiter - Convertor Implementation

The previously described transfer function and block diagrams of the RMS model described above, are identical or very similar to the implementation in the real convertor. However whilst the current limiter operates on the same principals its implementation is different. The voltage vectors are the primary calculation variables within the RMS model, simplifying implementation. In real convertors, it is difficult to determine if sudden changes in the AC wave are due to changes in voltage, phase or both.

A. FRT Strategy 1

From fig. 1, V_f can be indirectly measured from the measured output voltage (V_a *derived form* V_t) and the converter control signal (E_{1a}, E_{1b}, E_{1c}). Fig. 11 shows the block diagram for FRT strategy 1. The measured three phase output currents are used to determine the current magnitude ($\hat{I}_{abc}$) and this is compared to the current limit set-point ($\hat{I}_{limit}$) . If an over-current is detected (error > 0, from the limiter), then this error is fed to a PI controller to create an adjustment factor, (ΔV_F). The actual value of V_F is calculated from E_{1a} and V_a. This is scaled by the adjustment factor and the resultant value is then added to E_{1a} to determine the required converter voltage to limit the inductor voltage (V_F). The same ΔV_F is applied to all three phases.

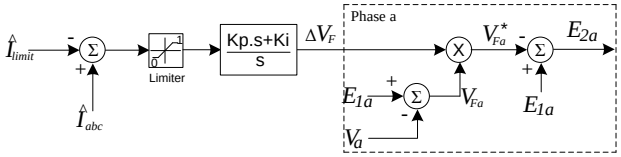

Fig. 11. Block diagram of FRT strategy 1

B. FRT Strategy 2

FRT strategy 1 uses the current magnitude ($\hat{I}_{abc}$), it can only operate effectively with a balanced three phase fault which limits its use. FRT strategy 2 focuses on limiting the current for each individual phase so that it can be used for asymmetric faults. Fig. 12 shows the block diagram of FRT Strategy 2 for phase a only. Phases b and c have similar structures. The voltage magnitude, ($\hat{V}_a$) of each cnverter phase is used to detect a fault, i.e. when $\hat{V}_a$ drops below 0.85pu in this case. When a fault is detected, V_F will be quickly reduced to zero to ensure the current will not increase above its limit. After a delay of one cycle the current is controlled back to its maximum value by activating the integral current controller. In addition, the phase current (I_a) can be used as an activated signal instead when other events such as vector shift occur, which may otherwise cause overcurrent.

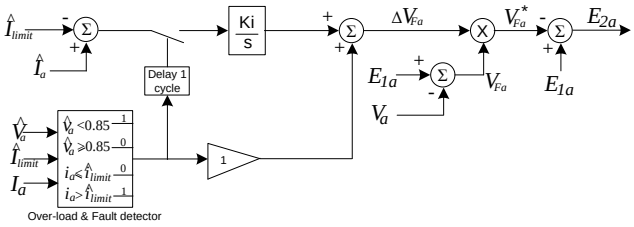

Fig. 12. Block diagram of FRT Strategy 2

V. Case Studies and Results

The proposed VSM control strategy has been verified through simulation studies using MATLAB/Simulink and lab tests. The case studies examined are a load step, a three-phase grid fault and a single-phase grid fault. To demonstrate the ability of the VSM to provide inertia support during a sudden load change the grid supply in this case is a 15kVA synchronous machine, to represent a weak supply. The simulation parameters are shown in Table I.

TABLE I Simulation Parameters

Parameters	Value
Grid frequency and voltage	50Hz 380Vrms
Line inductance	3mH
Inverter filter inductance and capacitance	2.3mH 10uF
Inverter rated	15KVA
FRT strategy1, K_p, K_i	10, 20
FRT strategy2, K_i	0.3

A. Load Step

The grid inertia is set to be 0.14 kgm^2 and three different VSM inertial values 0, 10 and 20 kgm^2 are used and compared to demonstrate the influence of this parameter.

Fig. 13 shows the grid frequency response to a step change in load and also shows the VSM active power injection. The 0.5pu load step is applied at 2 s. It can be seen that without the VSM system connected, the grid frequency drops quickly and by a significant value (10Hz). The VSM system is obviously able to enhance the response to the load change and maintain the grid frequency within its operating boundaries. The effect of the VSM inertia can clearly be seen

– higher inertia values reduce the rate of change of frequency due to the load impact as seen in Fig.13 (a).

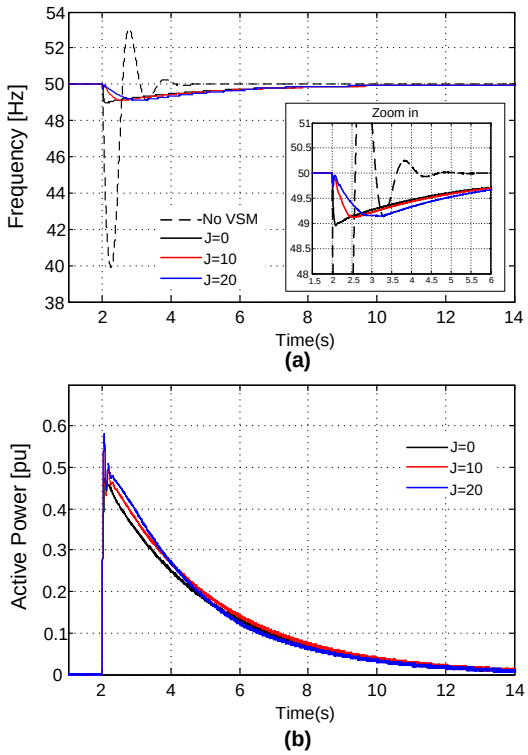

Fig. 13. 50% load step; (a) Grid frequency and (b) VSM output power

B. *Three Phase Balanced Fault*

The simulation results for the two FRT control strategies are compared in this section. A three-phase balanced fault with an impedance of 1.2 per phase is placed in parallel with the load.

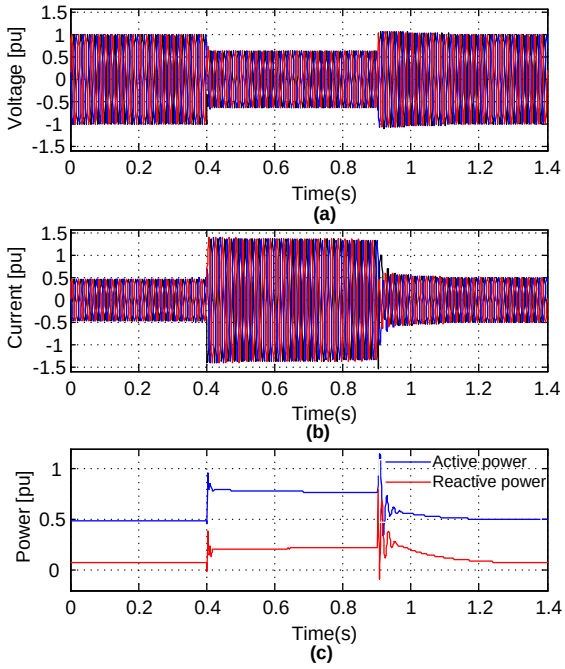

Fig. 14. Three phase balance fault for FRT strategy1; (a) VSM output voltage, (b) VSM inverter current and (c) VSM active and reactive power

The fault has a 500ms duration, occurring between 0.4s and 0.9s. The fault current limit is set to 1.3pu. Fig. 14 shows the response when using FRT strategy 1: the top and middle traces represent the three-phase output voltage and current of the inverter and the bottom presents the active and reactive powers.

It can be seen that when the fault occurs, the convertor current immediately rises up smoothly to the limit and is controlled at this. After the fault has been cleared, the controller is able to return the current back to its pre-fault value. However, there is an overshoot in the current level which is undesirable. The response of FRT strategy 2 as shown in Fig. 15 is similar, but in this case, the converter current reduces to zero before it rises to its limit value. When the fault is cleared, the converter current returns directly to its pre-fault value with no overshoot.

C. *Single Phase Fault*

A single-phase fault was applied to one phase with the same fault impedance as the previous section. The response of FRT strategy1 is shown in Fig. 16: in this case the converter current goes well above the limit (>1.7pu). This is because the control method assumes a balanced current, and the compensation term cannot be correctly added to the faulted phase only. However, the FRT strategy 2 manages to accurately control the fault current as shown in Fig17.

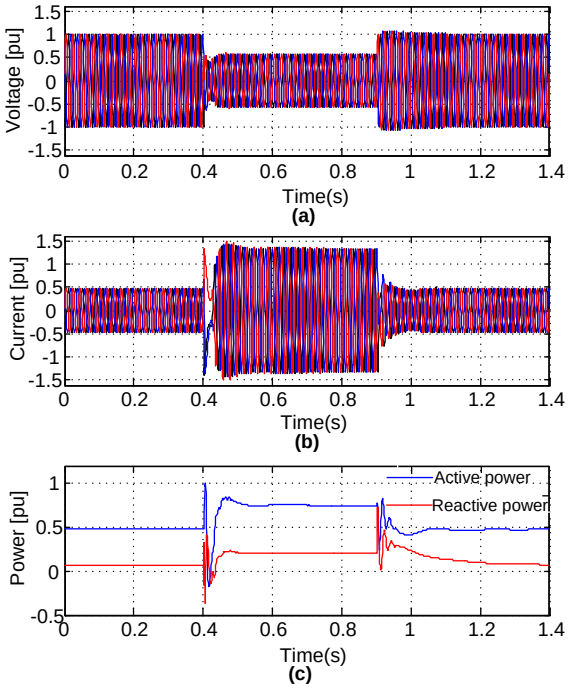

Fig. 15. Three phase balance fault for FRT strategy2; (a) VSM output voltage, (b) VSM inverter current and (c) VSM active and reactive power

VI. CONCLUSIONS

The algorithms and transfer function block diagrams listed in this paper and its accompanying papers in particular 2 [2], 4 [4] and 5 [5] demonstrate methods of implementing VSM in both real convertors and RMS models, which have been used in wider system models to demonstrate the benefits of this technology [6] [8].

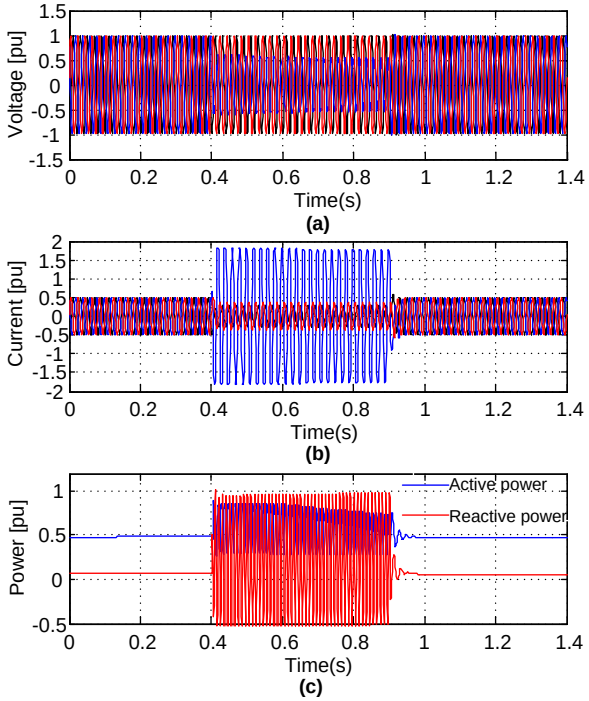

Fig. 16. Single phase fault for FRT strategy1; (a) VSM output voltage, (b) VSM inverter current and (c) VSM active and reactive power

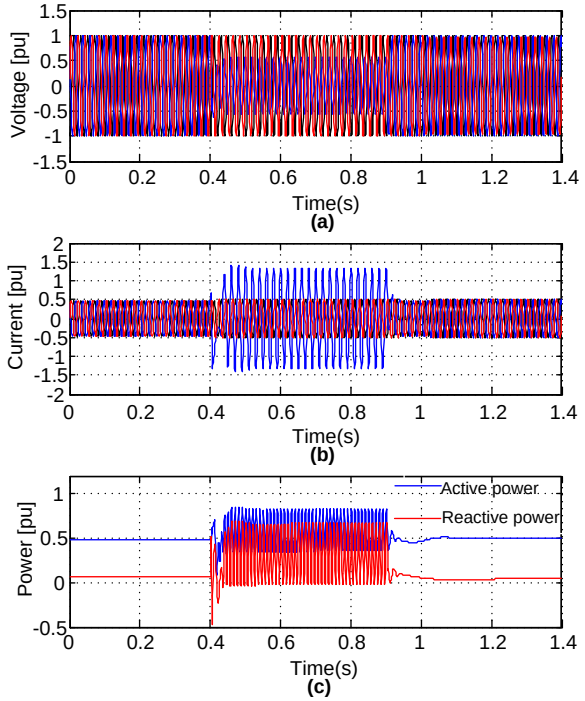

Fig. 17. Single phase fault for FRT strategy2; (a) VSM output voltage, (b) VSM inverter current and (c) VSM active and reactive power

The model and implementation of it have been developed from the original PowerFactory model presented in 2016 [2]. However, this model has been significantly improved with anti-wind up and dynamic braking added to the power limiter and voltage controller. Within PowerFactory the model can now be used with either a Static Generator element or PWM convertor which also models the DC bus and associated power components giving more accurate results.

Additional damping terms have been added to the RMS model to allow verification against lab convertor tests.

The power limiter presented has a constrained rapid angle change, limited to ±90 or ±180 Degrees, after which the design relies on the current limiter to control the output current. In practice further control may be required to manage the output power once the angle limit is reached. Manufacturers may wish to leave angle movement unconstrained, however further consideration may be required regarding this topic for reasons discussed in the body of this paper.

Contrary to the current GB GC [10] definition of Fault Ride Through, which requires generators to inject maximum reactive current during a fault, the implementation of the current limiter in the RMS model and convertor are aligned with the expectations of GC0100. This ensures the current limiter attempts to restore the voltage angle in a similar manor to the behavior of SM's, during faults.

VII. References

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